

## **NEPP Roadmaps, COTS, and Small Missions**

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#### **Acknowledgment:**

This work was sponsored by: NASA Office of Safety & Mission Assurance

### Open Access



Sundown at SCRIPPS Proton Therapy Center, Ken LaBel



## **Outline**

- NEPP Frame of Reference
- NEPP Tasks and Technology Selection
  - NEPP Technology Criteria
  - Selective Task "Roadmaps" including COTS
  - A Few Other Cool Tasks
- NEPP and Small Missions/Alternate "Assurance" Approaches
- Beyond Today
- Summary



## **Acronyms**

Acronym	Definition			
3D	Three Dimensional			
ACE	Absolute Contacting Encoder			
ADAS	Advanced Driver Assistance Systems			
ADC	Analog to Digital Converter			
AEC	Automotive Electronics Council			
AES	Advanced Encryption Standard			
AF	Air Force			
AF SMC	Air Force Space and Missile Systems Center			
AFRL	Air Force Research Laboratory			
AMS	Agile Mixed Signal			
ARM	ARM Holdings Public Limited Company			
Avalanche STT	Avalanche Technology Spin Transfer Torque			
Avaianene 311	Marconi Electronic Systems (MES) and British Aerospace			
BAE Systems	(BAe) merged to form BAE Systems			
BGA	Ball Grid Array			
вок	Body of Knowledge			
CAN	Controller Area Network			
CBRAM	Conductive Bridging Random Access Memory			
CGA	Column Grid Array			
CMOS	Complementary Metal Oxide Semiconductor			
CN	Xilinx ceramic flip-chip (CF and CN) packages are ceramic			
	column grid array (CCGA) packages			
CN/Kyocera	CN Package assembled at Kyocera			
Corp.	Corporation			
COTS	Commercial Off The Shelf			
CRC	Cyclic Redundancy Check			
CU	Control Unit			
Cu	Cu alloy			
DDR	Double Data Rate (DDR3 = Generation 3; DDR4 =			
DDK	Generation 4)			
DMA	Direct Memory Access			
DoD	Department of Defense			
DSP	Digital Signal Processing			
dSPI	Dynamic Signal Processing Instrument			
DTRA	Defense Threat Reduction Agency			
Dual Ch.	Dual Channel			
ECC	Error-Correcting Code			
EEE	Electrical, Electronic, and Electromechanical			
EMAC	Equipment Monitor And Control			
EMIB	Multi-die Interconnect Bridge			
ESA	European Space Agency			
eTimers	Event Timers			
FCCU	Fluidized Catalytic Cracking Unit			
FeRAM	Ferroelectric Random Access Memory			
FinFET	Fin Field Effect Transistor (the conducting channel is			
FDCA	wrapped by a thin silicon "fin")			
FPGA	Field Programmable Gate Array			
FPU	Floating Point Unit			
FY	Fiscal Year			
GaN	Gallium Nitride			
GAN GIT	Panasonic GaN GIT Eng Prototype Sample			

Acronym	Definition			
Gb	Gigabyte			
GIC	Global Industry Classification			
GPU	Graphics Processing Unit			
GSFC	Goddard Space Flight Center			
GSN	Goal Structured Notation			
GTH/GTY	Transceiver Type			
HALT	Highly Accelerated Life Test			
HAST	Highly Accelerated Stress Test			
HBM	High Bandwidth Memory			
HDIO	High Density Digital Input/Output			
HDR	High-Dynamic-Range			
HMC	Hybrid Memory Cube			
HP Labs	Hewlett-Packard Laboratories			
HPIO	High Performance Input/Output			
HPS	High Pressure Sodium			
1/0	input/output			
1/C 12C	<u> </u>			
i2MOS	Inter-Integrated Circuit			
	Microsemi second generation of Rad-Hard MOSFET			
IBM/GF	International Business Machines/Global Foundaries			
IC	Integrated Circuit			
IP	Intellectual Property			
JPEG	Joint Photographic Experts Group			
KB	Kilobyte			
LinFlex	Local Interconnect Network Flexible			
L-mem	Long-Memory			
LP	Low Power			
LVDS	Low-Voltage Differential Signaling			
LW HPS	Lightwatt High Pressure Sodium			
M/L BIST	Memory/Logic Built-In Self-Test			
MBSE	Model-Based Systems Engineering			
Mil/Aero	Military/Aerospace			
MIPI	Mobile Industry Processor Interface			
MMC	MultiMediaCard			
MMU	Memory Management Unit			
MOSFETs	Metal-Oxide-Semiconductor Field-Effect Transistors			
MPFE	Multiport Front-End			
MPU	Microprocessor Unit			
MRAM	Magnetic Random Access Memory			
NASA	National Aeronautics and Space Administration			
Navy Crane	Naval Surface Warfare Center, Crane, Indiana			
NEPP	NASA Electronic Parts and Packaging			
NGSP	Next Generation Space Processor			
NOR	·			
NRL	Not OR logic gate  Naval Research Laboratory			
NRO	United States Navy National Reconnaissance Office			
OCM	on-chip RAM			
PBGA				
	Plastic Ball Grid Array			
PCB	Printed Circuit Board			
PCle	Peripheral Component Interconnect Express			
PLL	Phase Locked Loop			
PoP	Package on Package			

Acronym	Definition			
PPAP	Production Part Approval Process			
Proc.	Processing			
PS-GTR	High Speed Bus Interface			
QFN	Quad Flat Pack No Lead			
QSPI	Serial Quad Input/Output			
R&D	Research and Development			
R&M	Reliability and Maintainability			
ReRAM	Resistive Random Access Memory			
RGB	Red, Green, and Blue			
RH	Radiation Hardened			
SAR	Successive-Approximation-Register			
SATA	Serial Advanced Technology Attachment			
SCU	Secondary Control Unit			
SD	Secure Digital			
SD/eMMC	Secure Digital embedded MultiMediaCard			
SD-HC	Secure Digital High Capacity			
SDIO	Secure Digital Input/Output			
SDM	Spatial-Division-Multiplexing			
SEE	Single Event Effect			
SERDES	Serializer/Deserializer			
Si	Silicon			
SiC	Silicon Carbide			
SK Hynix	SK Hynix Semiconductor Company			
SLU	Saint Louis University			
SMC	Air Force Space and Missile Systems Center			
SOA	Safe Operating Area			
soc	Systems on a Chip			
SPI	Serial Peripheral Interface			
STT	Avalanche Technology Spin Transfer Torque			
STT	Spin Transfer Torque			
TBD	To Be Determined			
TCM	Trellis Code Modulation			
Temp	Temperature			
THD+N	Total Harmonic Distortion Plus Noise			
T-Sensor	Temperature-Sensor			
TSMC	Taiwan Semiconductor Manufacturing Company			
UART	Universal Asynchronous Receiver/Transmitter			
USB	Universal Serial Bus			
VNAND	Vertical NAND			
WBG	Wide Band Gap			
WDT	Watchdog Timer			
WSTS	World Semiconductor Trade Statistics			



## **NEPP - Frame of Reference**

- EEE (electrical, electronic, and electromechanical) parts are:
  - All the things that are on printed circuit boards (PCB) inside of electronics boxes.



- Integrated Circuits (ICs or chips) like processors and memories as well as passives such as capacitors and resistors,
- Hybrid devices or multi-chip modules:
   Small packages that house multiple chips internally that are placed on the PCB, and,
- Connectors and wires used to send electrical or power signals between boards, boxes, or systems.

#### This does not include:

The PCB - NASA Workmanship Program responsibility.



PCB from Mars Rover Image courtesy NASA



Image courtesy BAE Systems

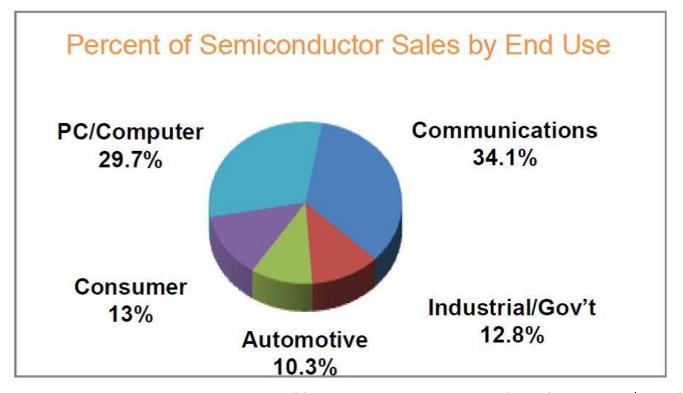


Image courtesy NASA



## **Motivational Factors**

#### 2015 Global Semiconductor Market: \$335 Billion



Source: WSTS End Use Report, 2015
Note: Military is <1% and is included in Industrial/Gov't

Military and Aerospace share is estimated at ~\$3.1B in 2015.

Aerospace is a small percentage of this amount.

In 1975, Military and Aerospace market share was ~\$50%! Conclusion: Mil/Aero community has to leverage.

There's no business model to go it alone!



# Technology Selection Criteria for NEPP Investigations

- The technologies should satisfy all or most of the following criteria:
  - Wide applicability,
  - Product level or in productization, and,
  - No distinction: COTS to high-reliability aerospace.
- In general, we avoid:
  - Laboratory technologies, e.g., <TRL3,</li>
  - Limited application devices with certain exceptions (critical application or NASA center specialization).
- Note: Partnering arrangements with other organizations preferred.
  - Industry examples: Microsemi, Xilinx, Altera (Intel), TI
  - Other U.S. Government: AF SMC, AFRL, DTRA, Navy Crane, NRO, NRL, etc...



## **NEPP** – Deeper Dive for Tasks

- NEPP has multiple rationale for evaluating a specific device or technology:
  - If the device/technology has the potential for widespread usage across the Agency,
  - If the device has true enabling characteristics for next generation mission needs, or,
  - As a means of gathering assurance information for future mission insertion or screening/qualification methods.
- The following roadmap charts are focused on the advanced power and digital electronics regimes.
  - NEPP has efforts not being presented on connectors, capacitors, and other categories.
    - Ex. Cu wirebonds is an active future area currently in discussion on tasks.



# **Technology Investigations: Sample Roadmaps Discussion**

#### Caveats:

- Guidelines are often a product of technology evaluation tasks.
- Only major product categories shown.

#### Notes:

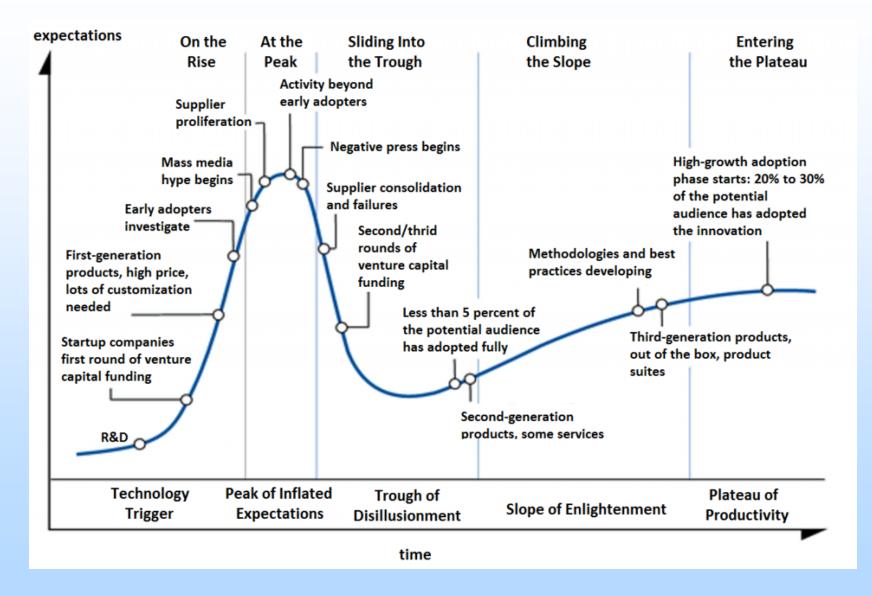
- Separate CMOS roadmap not included.
  - NEPP leverages samples from ongoing DoD and/or commercial sources.
  - 1xnm is current target (IBM/GF, INTEL, Samsung, TSMC).
- "Reliability testing" may include product and/or package testing.
- "Body of Knowledge" BOK document provides a snapshot status on a technology (manufacturing, reliability, radiation) and identifies gaps for future work.

## Technology areas not on NEPP Roadmap, but under consideration include:

- Electro-optics (fiber optics),
- Advanced analog and mixed-signal devices,
- Imaging sensors,
- Modeling and simulation,
- High-speed communication (SERDES, fast data switches), and,
- Adjunct processors (eg., graphics, signal processing).

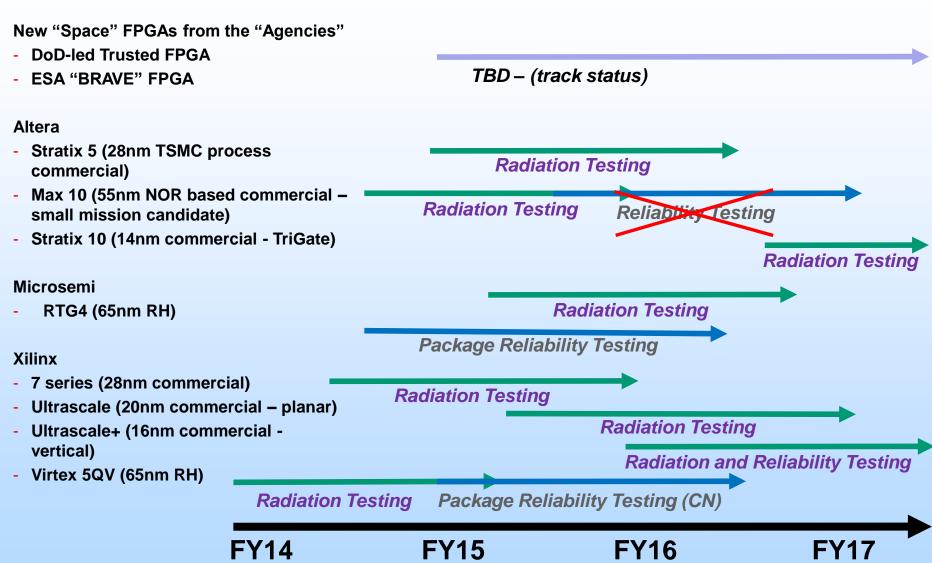


## **Gartner Hype Cycle Concept**



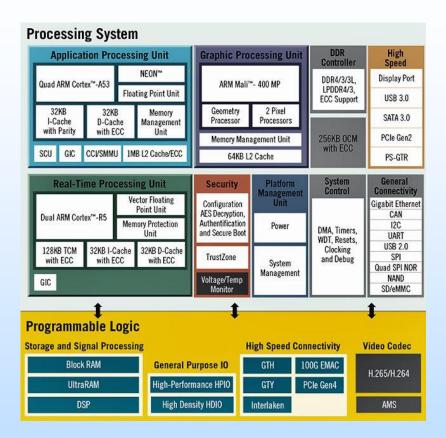


## Field Programmable Gate Arrays (FPGAs)





## **Next Generation "FPGAs"?**



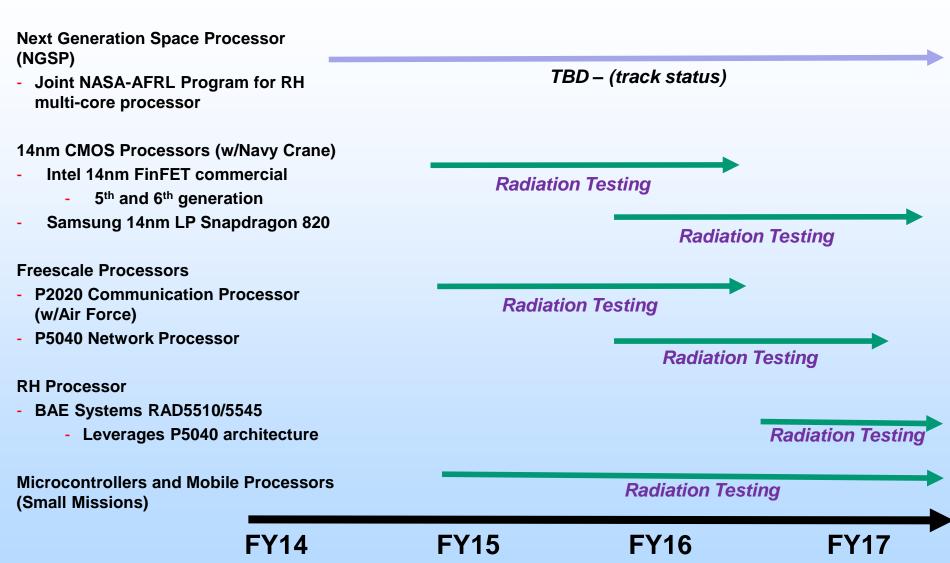
From Xilinx.com



From Altera.com



## **Advanced Processors**



Note: Future considerations include adding Graphics Processing Units (GPUs) to NEPP Roadmap in FY17.



## **Commercial Memory Technology**

- collaborative with Navy Crane

#### Other

- MRAM (Avalanche STT, other)
- FeRAM

#### TBD – (track status/test when available)

#### Resistive

- CBRAM (Adesto)
- ReRAM (Panasonic)
- ReRAM (Tezzaron)
- TBD (HP Labs, others)

Radiation and Reliability Testing

Radiation and Reliability Testing

45nm options

Radiation and Reliability Testing

TBD – (track status)

#### **DDR**

- Intelligent Memory (robust cell twinning)
- 1xnm DDR3, DDR4, LP (TBD)

#### Hybrid or wide I/O

HMC, HBM, Wide I/O

#### **Radiation Testing**

Radiation and Reliability Testing

TBD – (track status or test)

#### **FLASH**

- Samsung VNAND (gen 1 and 2)
- Micron 16nm planar
- Micron 3D
- SK Hynix 3D, other commercial

Radiation and Reliability Testing

Radiation and Reliability Testing

Radiation and Reliability Testing

Radiation and Reliability Testing

FY14

**FY15** 

**FY16** 

FY17



# Alternate Grade Electronics: Automotive

- NEPP has three goals for automotive electronics efforts
  - Determine exactly what:"automotive grade" does or does not entail.
    - Includes understanding:
      - Automotive Electronics Council (AEC) documents, and,
      - Manufacturer Production Part Approval Process (PPAP).
  - Perform "snapshot" screening and testing on representative automotive grade electronics.
  - Explore application of resilient automotive electronics system designs for space purposes.

Automotive application constraints or standard compliance	To be implemented and managed at different levels				
	Audio IP	SoC	Application firmware/ software	РСВ	
Noisy ground(s) voltage	Common mode rejection			Passive components' accuracy	
Audio perception and spatialization	THD+N, gain mismatch, Pop-up Noise	SoC routing resistance	Processing, starting and stopping sequences	Application Schematics consideration	
Security	Primary diagnostic circuitry	Redundant audio interface	audio diagnostic firmware	Protection circuitry	
High Temperature operation (AEC-Q100 Grade 0/1 qualification)	High performance at junction Temperature -40 °C to 125 °C	Package thermal dissipation consideration		PCB material and component soldering technology consideration	

http://www.design-reuse.com/ news\_img/20141209\_2.jpg



## **Small Missions/ Automotive**



- Small missions (Class D, CubeSat2 documents)
- System on a chip (SOC) single event effects (SEE) guideline
- Board-level proton test guideline

#### **Small Mission Commodities**

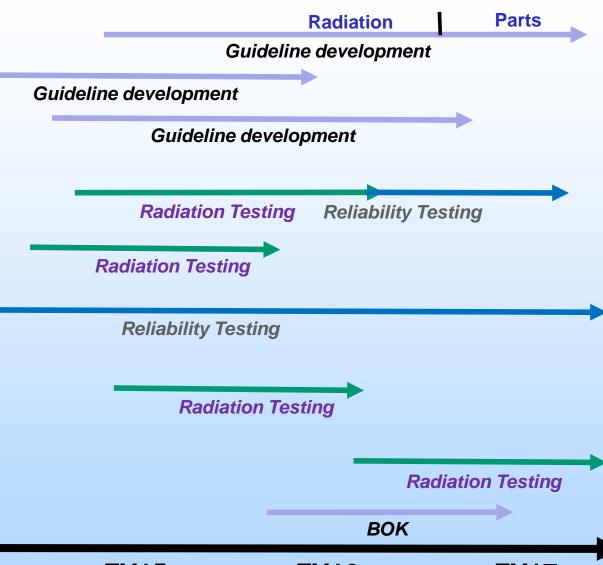
- See commodities roadmaps for processors, memory, FPGAs, power
- CubeSat Star Tracker

#### **Automotive grade electronics**

- Multiple classes of electronics (passives, actives, ICs)
  - NASA and Navy Crane
- Freescale MPC56XX

#### Alternate system tests

- Automotive resilience system tests
- Use of board-level testing for screening and qualification - BOK



**FY14** 

**FY15** 

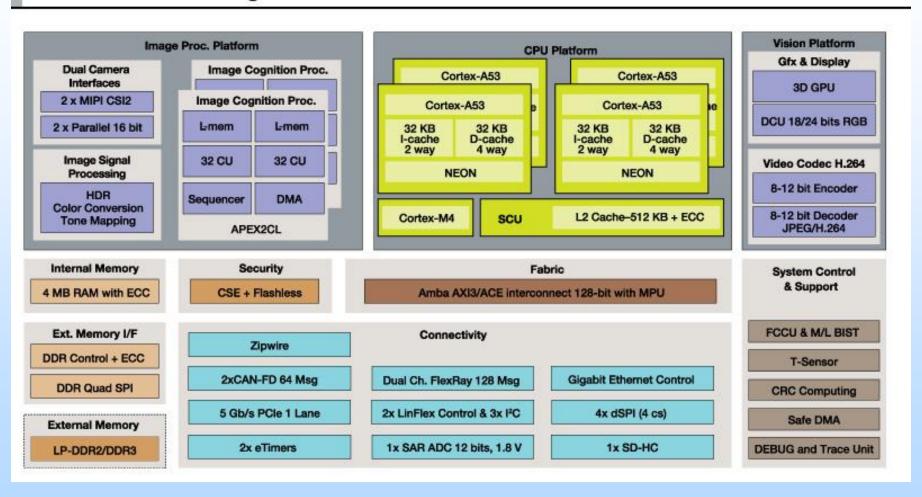
**FY16** 

FY1:



# Automotive Advanced Driver Assistance Systems (ADAS) for Space?

#### S32V234 Block Diagram



From Freescale.com



## Power and Wide Band Gap (WBG) Devices

#### Si MOSFETs - Rad Hardened

- Microsemi i2MOS
- Infineon superjunction 100 V, 600 V (target)

## Radiation Testing

**Radiation Testing** 

(track status)

#### Si Schottky Diodes

 Multiple vendors, reverse voltage ratings, and forward current ratings

#### **Radiation Testing**

Safe Operating Area (SOA) Guideline Development

**BOK** 

#### **SiC**

- Body of Knowledge (BOK) document (knowledge and gap analysis)
- Cree Gen 1-3
- Collaboration w "hardening" efforts
- Baseline diodes
- Logic devices

#### Radiation and Reliability Testing

Radiation Testing

**Radiation Testing** 

**Radiation Testing** 

#### GaN

- EPC 2012 (Gen3) and 8000 Series
- GaNSystems GS61008 and GS66508 commercial
- Panasonic PGA26E19BA (Gan SIT)
- Thransphorm TPH3202PD (Cascode)
- Freebird Semiconductor\_

Radiation Testing Reliability Testing

Radiation Testing

Reliability Testing

Radiation Testing

Reliability Testing

Radiation Testing

Reliability Testing

Radiation Testing

**FY14** 

FY15

**FY16** 

FY17



## IC Packaging

Reliability Testing

## High Density, Non-hermetic Column Grid Array (CGA)

- Xilinx CN/Kyocera Daisy Chain
- Microsemi Daisy Chain

## Reliability Testing Reliability Testing

## HALT Methodology/Qualification

- HALT/HAST comparison
- Plastic BGA matrix

#### **Area Array Column**

- Selection guide

#### **Thermal Interface Materials**

- Selection guide

## PBGA Thermal Cycle Evaluation

2.5/3D Packaging QFN package reliability



Reliability Testing

Guideline development

BOK Reliability Testing

Reliability Testing

Reliability Testing

**FY14** 

**FY15** 

**FY16** 

FY17



## A Few Other Cool Tasks...

- CubeSat mission success/failure root cause analysis
  - Grant to Saint Louis University
- Using a model-based systems engineering (MBSE) approach to radiation assurance
  - Grant to Vanderbilt
  - Co-sponsored by NASA Reliability and Maintainability Program
  - Uses a tool called "Goal Structured Notation"
- Keeping the CRÈME website alive
  - Support to Vanderbilt
  - Just standard maintenance and operation, no upgrades
- Proton test facilities
  - See poster on 6/14.



## **Beyond Today – Sample Challenges**

- Complexity and sub-microscopic feature size issues for inspection, screening, device preparation, and test
  - 2.5/3D Packages/ICs
  - Package on Package (PoP) Commercial Devices
  - FPGAs combined with an SOC
  - Cu Wirebonds
  - 14 nm and below feature sizes
  - ESD susceptibility
  - Trust
- Assurance
  - Automotive and catalog commercial EEE parts?
  - Increasing risk with a worldwide supplier base
    - Traceability
    - Change control
    - Screening?
  - Consolidation
    - What if the only source left is in an inhospitable or unauditable part of the world?



## NEPP and Small Missions/ Alternate "Assurance" Approaches

#### Sample Current Efforts

- Radiation Hardness Assurance for Small Missions
- Root Cause Analysis and Success Tracking of CubeSats (Prof. Michael Swartwout/SLU) – we're looking for possible low hanging fruit for university-class CubeSats
- Model-Based Missions Assurance for CubeSats:
  - 1st task is a Goal Structured Notation (GSN) exemplar of a CubeSat board this is joint with the NASA Reliability and Maintainability (R&M) Program
- Board-level proton test guideline
- Automotive grade EEE parts
- CubeSat parts database both kit manufacturers and usage within NASA
- Multiple COTS evaluation tasks relevant to CubeSat usage including microcontrollers, memories star trackers, power devices, and FPGAs...

#### Future considerations

- COTS, COTS (and alternate grade electronics)
- Continue and extend R&M collaboration (Bayesian methods, anyone?)
- EEE Parts Best Practices for Small Missions



## **Summary and Comments**

- NEPP Roadmaps and Tasks are constantly evolving as technology and products become available.
  - Like all technology roadmaps, NEPP's is limited to funding and resource availability.
    - Many other efforts are not being shown today (60+ tasks total)
  - Partnering is the key:
    - Government,
    - · Industry, and,
    - University.
- We look forward to further opportunities to partner.

https://nepp.nasa.gov